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DISCRETE ACTIVITY INDICATOR SYSTEM

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ABSTRACT

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A discrete activity indicator system processes 768 discrete signal inputs and presents information to a computer only when a change in an input occurs. Resolution time of the system is approximately 1.2 milliseconds for 1000 discrete inputs.

A basic clock in the system drives a functional clock which, in turn, drives a binary counter and six eight-phase drivers in parallel. Each eight-phase driver operates a 128-way current-steering switch, which sequentially interrogates the cores of a 128-bit memory bank. If a change occurs in a discrete signal input (from 0 to 28 V dc or 28 to 0 V dc), an output is obtained from the associated memory core (when the core is interrogated) and is applied to a sense amplifier. The outputs from the sense amplifier and the binary counter are then applied to a system register for transfer to the computer. These signals allow the computer to determine which discrete signal changed and the direction of the change. When a change occurs, a priority-interrupt circuit stops the interrogation until the computer processes the information. After the information is processed, a clock-start multivibrator allows the interrogation to resume.

The power requirement for the system is reduced 75 percent by using a ground commutator to turn on the discrete drivers of the memory in groups of 16 when each particular group is being interrogated.

Positive synchronization between the binary counter and the current-steering switches is provided by a binary synchronizer.

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DISCRETE ACTIVITY INDICATOR SYSTEM

SUMMARY

The operation of a discrete activity indicator system is described. The discrete activity indicator is a special purpose device designed to gather and process discrete data for presentation to a computer. It relieves the computer of scanning, addressing, and the many other tasks associated with data acquisition, and enables the computer to handle more logic and decision-making functions.

SECTION I. INTRODUCTION

In acquiring and processing all the discrete functions (opening and closing of relays, for instance) of a space vehicle or other complex system, the associated computer is rendered more useful by the addition of a scanning device between the system and the computer. This device, or activity indicator, repeatedly scans all its inputs and presents an output to the computer only when a change has occurred since the previous scan. This preprocessing of the input signals frees the computer for logic and decision-making functions.

The discrete activity indicator described here is a special purpose device for use with the RCA-110 computer. A ferrite toroidal core is used as the basic element for both logic and memory functions. A general system description is given first and is followed by more detailed descriptions of individual units. Since the circuits used are fairly common, emphasis is placed on the manner in which the circuits are utilized rather than on the circuit details.

The author attributes the original study of a binary counter used in the system to Milton Rosenberg of Electronic Memories, Inc. The author also acknowledges the invaluable contributions of Gayle Berryman, Curtis Rister, and John Waldrop to the conversion of the idea into a reality.

SECTION II. SYSTEM DESCRIPTION

The activity indicator system (Fig. 1) receives 768 discrete signal inputs, which are evenly apportioned among six memory units (128 inputs per unit). The scan rate of the system is 100 kHz and the six memory units are scanned in parallel to increase the effective scan rate. Resolution time of the system is about 1.2 ms for 1000 discrete inputs.

System scanning is controlled primarily by a basic clock which is an astable multivibrator capable of driving other logic and blocking-oscillator units without intermediate amplification stages. The output of the basic clock triggers a blocking-oscillator clock stopper.

Since the computer cannot process information at the scanning rate of the system, the clock stopper stops the scanning when a change in a discrete signal input is detected. This allows time for the information to be processed by the computer. After the computer processes the information, the scanning is resumed. The output of the clock stopper drives a functional clock.

The functional clock is essentially a four-phase driver that produces four sequential outputs from a single input. In the order of their time sequence and in typical computer format, the outputs are labeled α, β, γ, and δ.

The α pulse from the functional clock drives a binary counter. The β pulse resets the top cores of the binary counter, drives an eight-phase driver of the first memory unit, and triggers five blocking oscillators. Each of these blocking oscillators, in turn, drives an eight-phase driver (one in each of the five remaining memory units). The γ pulse of the clock is unused. The δ pulse resets the flux around the small aperture in each core of the binary counter.

Since six memory units are operated in parallel, only one binary counter is needed for the system. This transistorized seven-stage counter requires four pulses to provide one output in a nondestructive read mode. The α, β, and δ pulses are supplied by the functional clock. The fourth pulse, the read pulse, is a β pulse that has been delayed by propagation through the eight-phase driver, current-steering switch, memory circuit, sense amplifier, and read driver. The read pulse,

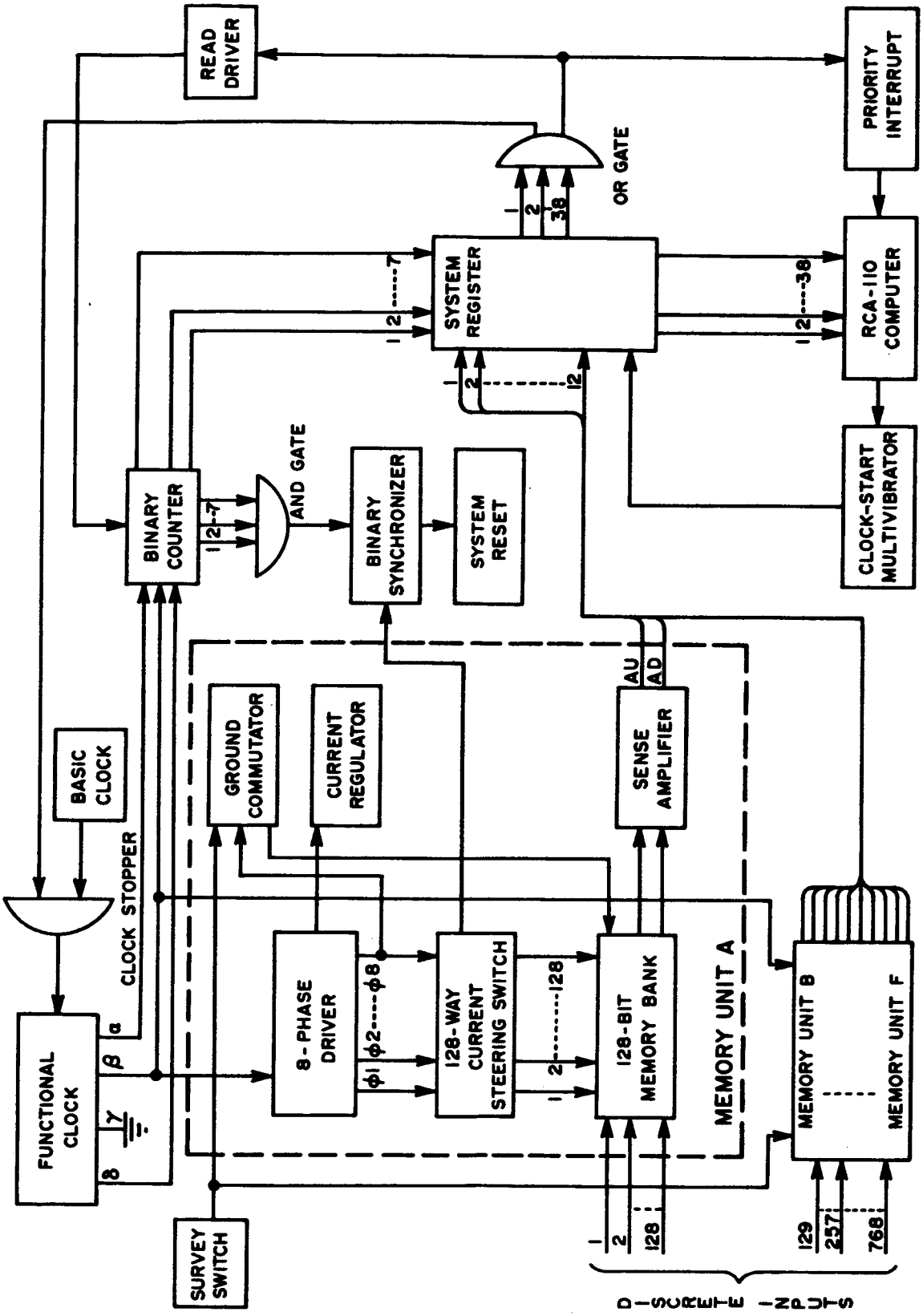

FIGURE 1. SYSTEM BLOCK DIAGRAM

which nearly coincides with γ time and is present only when a change in a discrete signal occurs, gates the output of the counter to a system register. An output is provided to a multilegged AND gate from each binary stage of the counter. The output of this AND gate and an output of the 128-way current-steering switch are fed to a binary synchronizer. The binary synchronizer is essentially a sequential AND gate, the output of which drives a system reset. If the inputs to the binary synchronizer are out of sequence, the system reset is triggered and returns the system to the starting point of the scanning process.

Since it is very difficult to drive more than 25 cores of a current-steering switch from one source and still maintain good current definition, an eight-phase driver is employed to operate the 128-way current-steering switch.

The eight-phase driver is similar to the four-phase driver. It has eight sequential outputs, each of which drives 16 cores of the current-steering switch. The last phase of the eight-phase driver also operates a blocking oscillator which, in turn, drives a ground commutator.

A current regulator is employed to produce the desired current waveform from the eight-phase driver.

The 128-way current-steering switch is a stepping register that sequentially interrogates the cores in a 128-bit memory bank. The memory bank consists of 128 small cores. Each core has an external input from a discrete source and from an interrogation line. To reduce the number of interrogation lines required, a single interrogation pulse simultaneously checks two cores for changes in the respective discrete signal inputs. One core is checked to determine if a discrete signal turned on (up-going signal), while an adjacent core is checked to determine if a discrete signal turned off (down-going signal). Since it is impractical to operate two cores simultaneously on one sense or output winding, one sense winding links all odd cores and another links all even cores.

Each core of the memory is driven by a discrete driver. If a condition existed in which the discrete drivers in all memory units were on at the same time and remained on, the power required for the system would be excessive. The ground commutator eliminates this possibility by turning on the discrete drivers in groups of 16. This

results in a power reduction of 75 percent. Two groups in each memory unit are turned on simultaneously. The switching logic ensures that no memory core is interrogated while its discrete driver is being turned on.

The output of the memory bank is fed to a sense amplifier, where the up-going and down-going signals are separated and applied to the system register.

Outputs from this register are then applied to the computer and to an OR gate. The output of the OR gate drives the read driver, the clock stopper, and a priority interrupt. The read driver supplies the read pulse to the binary counter, and the clock stopper prevents the output of the basic clock from reaching the functional clock when a change is detected in a discrete signal input. The priority interrupt informs the computer that new information is in the system register and that this information is ready to be written into one of the computer registers.

After processing the received information, the computer supplies a pulse to a clock-start multivibrator, which resets the system register and removes the OR gate signal, allowing the system to resume scanning.

A survey switch is provided to allow the operator to observe any condition that exists in all discrete inputs at any one time.

SECTION III. DETAILED TECHNICAL DESCRIPTION

A. BASIC CLOCK

The basic clock is an astable multivibrator utilizing Fairchild micro-logic circuits. These circuits were chosen for their high-frequency capabilities and their ability to drive other logic and blocking oscillator units without requiring intermediate amplification stages. The output of the basic clock, approximately 400 kHz, triggers the blocking oscillator clock stopper which, in turn, drives the functional clock.

B. FUNCTIONAL CLOCK

The functional clock is essentially a four-phase driver consisting of four blocking oscillators with transformers of square-loop core material. (Refer to Figure 2 for a typical N-way phase driver.) These blocking oscillators are driven from the same source and are connected in such a manner that only one blocking oscillator is triggered for each input pulse. The output of each blocking oscillator resets the core of the next blocking oscillator, preparing it to be triggered on the subsequent input pulse.

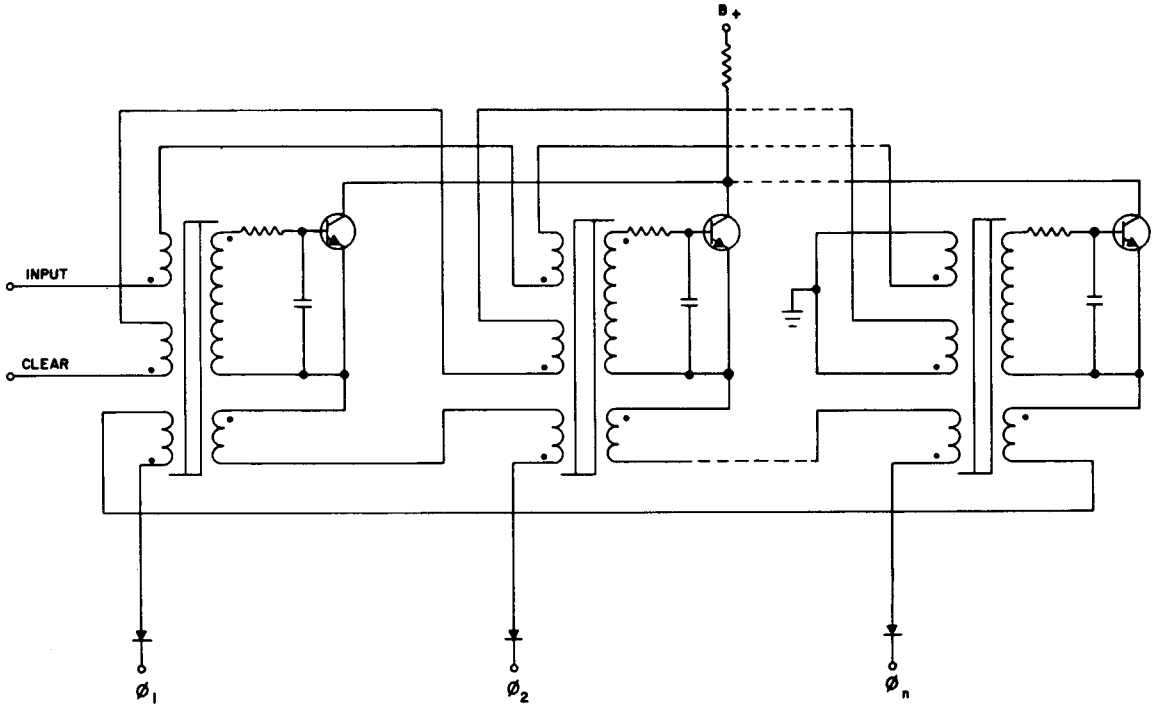

FIGURE 2. N-WAY PHASE DRIVER

Four sequential outputs are produced by the functional clock: α, β, γ, and δ. The α pulse drives the binary counter. The β pulse resets the top cores of the binary counter, drives the eight-phase driver of the first memory unit, and triggers five blocking oscillators. Each of these blocking oscillators, in turn, drives an eight-phase driver (one in each of the five remaining memory units). The γ pulse of the clock is unused. The δ pulse resets the small apertures of the binary counter cores. Thus, each unit in the system is internally synchronized with the β pulse from the functional clock.

C. BINARY COUNTER

The binary counter (Fig. 3) is a transistorized, seven-stage counter that uses multi-aperture cores to effect a nondestructive readout. The cores are made of a ferrite material which has a square hysteresis-loop characteristic. Since each memory unit has 128 inputs, and six units operate in parallel, only one counter of 128 is needed for the complete system.

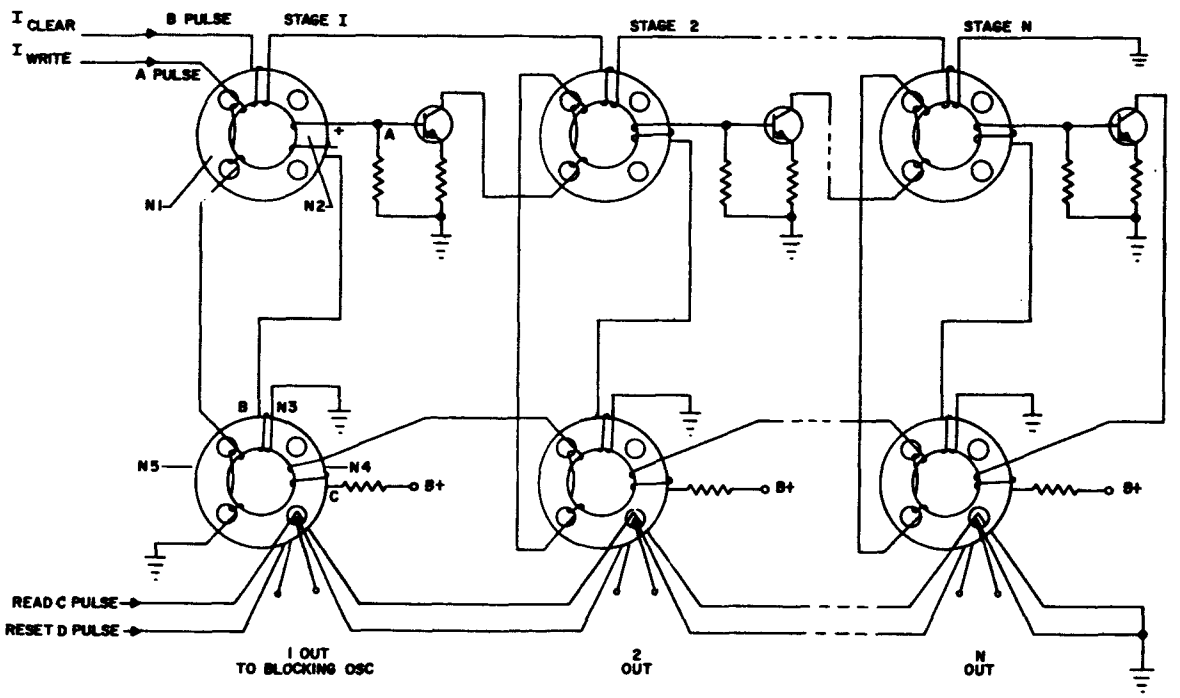

FIGURE 3. BINARY COUNTER

Four pulses in sequence are required by the counter to provide one output in the nondestructive read mode. In the order of their time sequence, the pulses are labeled A, B, C, and D. The C pulse for the binary counter is derived from the β pulse of the functional clock. The β pulse is delayed by the propagation through the eight-phase driver, current-steering switch β, memory circuit, sense amplifier, and read driver. When the β pulse reaches the binary counter, it very nearly coincides with γ time. The C pulse is present only when there has been a change in a discrete input. The A, B, and D pulses are actually the functional clock α, β, and δ pulses, respectively.

In reference to Figure 3, assume that the flux in all cores has been switched to "zero" in a counterclockwise direction. The first A pulse switches flux in a clockwise direction about the inner circumference of both cores of stage 1. The two cores are identical and the same amount of flux is switched in each core since they are driven from the same source. During switching, a positive voltage appears across winding N2 and a negative voltage appears across winding N3. Since more turns are on winding N3, the net voltage at point A is negative, keeping the transistor turned off. The B pulse then switches the top cores of all seven stages back to the "zero" state. Thus, at the end of B time, the flux in the bottom core of stage 1 has been switched about the inner circumference in a clockwise direction ("one" state), and the top core is in a "zero" state.

When the A pulse occurs again, the top core of stage 1 is switched to a "one" state, and a positive voltage is again generated across winding N2 during switching. The bottom core cannot be switched, since it was previously set to a "one" state; hence, no voltage appears across winding N3. This causes a net positive voltage to appear at the base of the transistor. The transistor circuit has basically a blocking oscillator configuration with the bottom core; and once the transistor is triggered, the operation is self-sustaining. As current begins to flow in the collector of the transistor, flux in the top and bottom cores of stage 2 is switched to a "one" state. At the same time, flux in the bottom core of stage 1 is switched to a "zero" state because of the blocking-oscillator action. The B pulse then comes in and resets the top cores to a "zero" state. At the end of the second B pulse, both cores of stage 1 are in a "zero" state, but the bottom core of stage 2 is in a "one" state. The binary count is held and read out from the bottom core.

By applying this process successively, the frequency of the transistor pulses of each succeeding stage are one-half the frequency of the preceding stage. Consequently, the period of time that "ones" and "zeros" remain in the bottom core of any one stage is half the period of time that "ones" and "zeros" remain in the bottom core of every succeeding stage.

Information is obtained from the bottom cores by using the smaller aperture in each core along with C and D pulses. As shown in Figure 4, the flux around the small aperture is changed during the

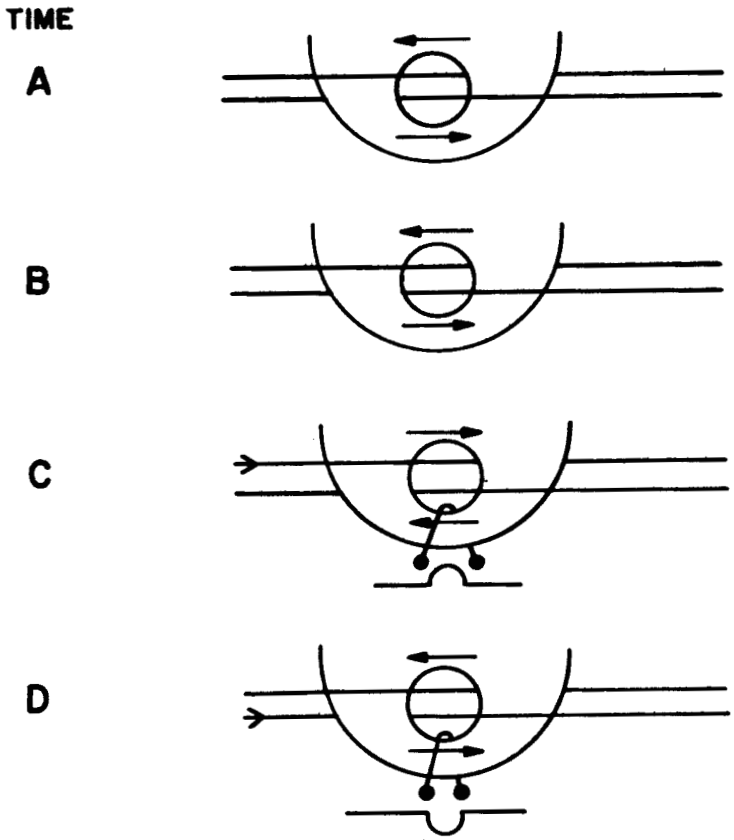

FIGURE 4. FLUX CONDITION AROUND SMALL APERTURE AFTER EACH DRIVING PULSE

A pulse; however, the C pulse switches only the flux about the smaller aperture and produces an output voltage when a "one" has been written into the bottom core. The D pulse switches the flux back to the "one" state. This means that a "one" is always seen at the output for each C pulse unless the transistor of that particular stage has set the bottom core to a "zero" state. When the bottom core is in a "zero" state, the flux lines on each side of the aperture are parallel in the same direction. Therefore, a C pulse cannot switch the flux around the aperture without switching the flux around the whole core, and the magnetomotive force of the C pulse is not sufficient to do this. The voltage pulse from the output windings triggers a blocking oscillator for an output to the register.

The binary output is gated to the register when a change in a discrete input has occurred. An output is provided from the collector of each binary stage transistor. These outputs are needed as inputs to a multilegged AND gate to obtain synchronizing pulses.

D. MEMORY UNITS

The six memory units of the system are identical; therefore, the circuitry of only one unit is described. Each memory unit contains an eight-phase driver, a current regulator, a 128-way current-steering switch, a memory bank, a ground commutator, and a sense amplifier.

1. Eight-Phase Driver. Since it is very difficult to drive more than 25 cores of the current-steering switch from one source and still maintain good current definition, an eight-phase driver is employed to drive the 128-way current-steering switch.

The eight-phase driver is similar in operation to the functional clock and is triggered by the β pulse from the functional clock. The eight-phase driver provides eight outputs in sequence to the 128-way current-steering switch. The last phase of each eight-phase driver also triggers a blocking oscillator. This blocking oscillator, in turn, drives the ground commutator.

2. Current Regulator. The current regulator is employed to produce the desired current waveform from the eight-phase driver. The current regulator consists of two silicon power transistors connected in parallel for class A operation. They are driven in a Darlington configuration from a voltage source derived from a zener diode.

3. 128-Way Current-Steering Switch. The 128-way current-steering switch (Refs. 1, 2, and 3) is similar to a conventional shift register used as a ring counter. The important difference is that the advance current in the current-steering switch is the same current steered through the cores of the 128-bit memory bank.

The 128-way current-steering switch is a stepping register that delivers interrogation currents in sequence to the cores of the 128-bit memory bank. Each phase of the eight-phase driver operates a group of 16 cores in the current-steering switch as shown in the Table.

To avoid confusion, the operation of the current-steering switch is explained using the simplified schematic of a two-phase, N-way current-steering switch shown in Figure 5.

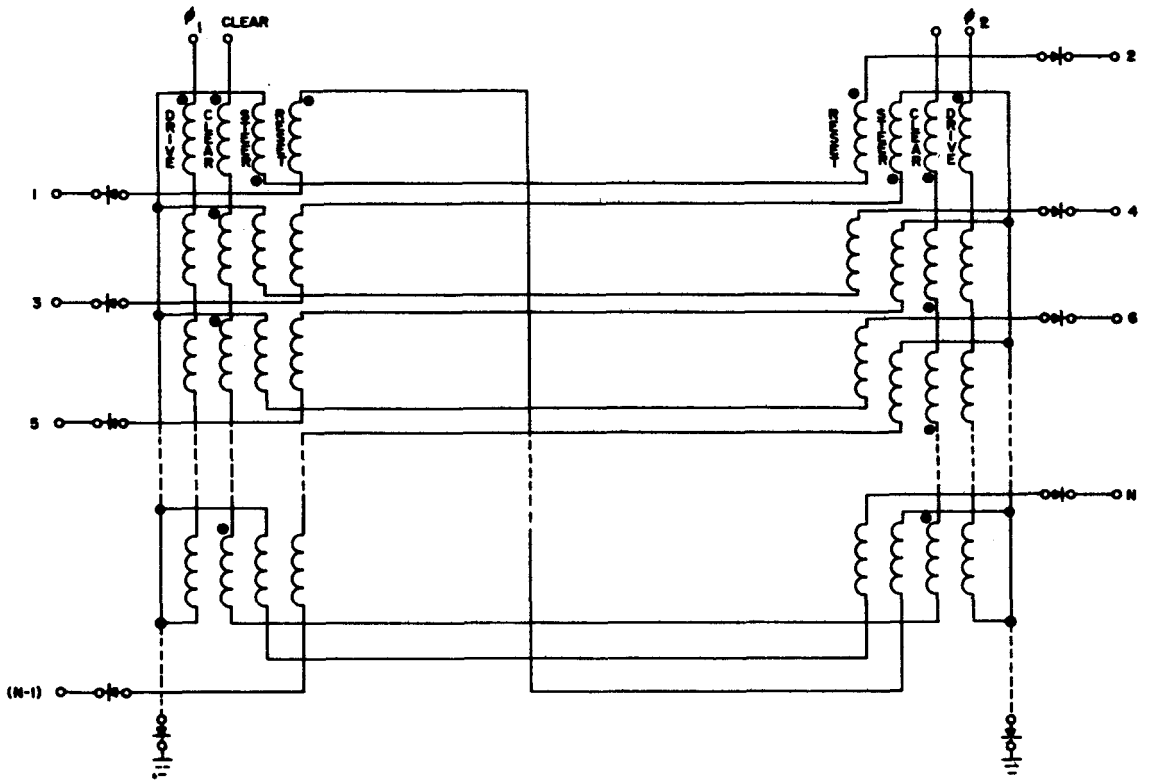

FIGURE 5. N-WAY CURRENT-STEERING SWITCH

Table. Eight-Phase Driver Loads

	Phase							
	2	3	4	5	6	7	8	1
Current-Steering-Switch Cores	1	2	3	4	5	6	7	8
	9	10	11	12	13	14	15	16
	17	18	19	20	21	22	23	24
	25	26	27	28	29	30	31	32
	33	34	35	36	37	38	39	40
	41	42	43	44	45	46	47	48
	49	50	51	52	53	54	55	56
	57	58	59	60	61	62	63	64
	65	66	67	68	69	70	71	72
	73	74	75	76	77	78	79	80
	81	82	83	84	85	86	87	88
	89	90	91	92	93	94	95	96
	97	98	99	100	101	102	103	104
	105	106	107	108	109	110	111	112
	113	114	115	116	117	118	119	120
	121	122	123	124	125	126	127	128

Initially all cores, except the N core, are switched; therefore, drive current flowing through the Ø2 windings switches only the N core. When the N core switches, a voltage is induced in the N-core output winding. This voltage causes a current to flow through a winding of core No. 1 (to reset that core) and through diode No. 1 to interrogate two cores of the 128-bit memory bank. To ensure that no leakage current flows through other output lines when core No. 1 is reset, enough turns are placed in the steer windings of core No. 1 to keep the common bus below ground potential. As a result, the current flows entirely in the selected branch. When the drive current from the eight-phase driver flows through the Ø1 windings, core No. 1 produces an output which resets core No. 2 and interrogates two additional cores of the 128-bit memory bank.

To achieve complete turnover of the cores, there must be more turns on the drive winding than there are on the steer windings, because the steer current opposes the effect of the driving current.

Since the switching and resetting operations of the current-steering switch cores would produce bidirectional signals in the memory, a unidirectional switch was developed. The most effective means to obtain a unidirectional switch is to insert a diode in each output circuit. With this arrangement, current flows from the current-steering switch into the memory bank in only one direction. Since this back-biased diode prevents any loading during reset, only a small amount of power is needed. The diode is highly reliable in this mode of operation since the voltages in the output are very low and the diode does not require a large back resistance.

The duration of the drive-current pulse from the eight-phase driver is by necessity longer than that required to switch a core of the current-steering switch. Therefore, after a core has been switched, the drive current is divided evenly among the switching windings of other cores in that group, until the drive current is removed. This current division constitutes noise to the memory. The noise currents are minimized substantially by inserting a diode in the line from the phase bus to ground. Since the impedance of the conducting diode is much less than that of the combination of parallel lines in the memory bank, the diode provides a current sink, or shunt, to ground.

4. Memory Bank. Each memory unit contains a 128-bit memory bank composed of 128 ferrite toroidal cores. A simplified schematic of a memory bank is shown in Figure 6. Each core has two interrogation windings, a discrete signal input winding, and an output (or sense) winding.

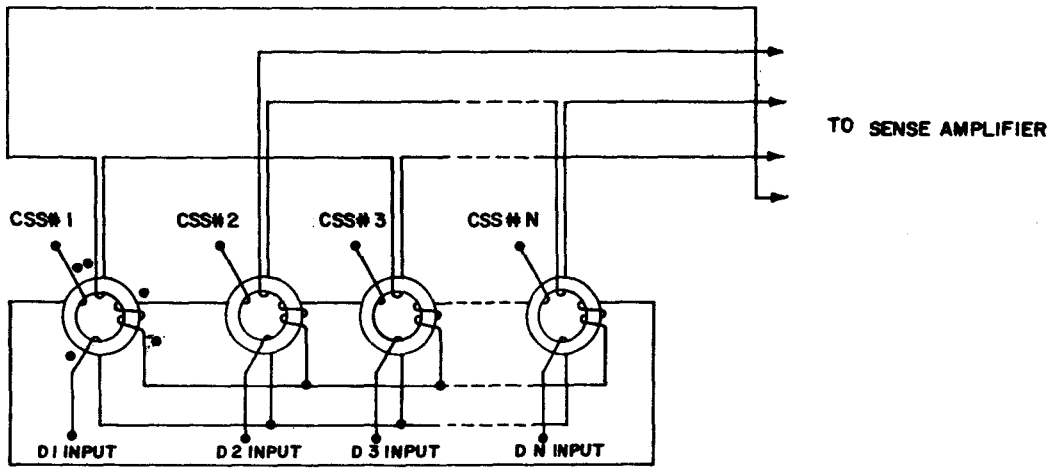

FIGURE 6. MEMORY BANK

The two interrogation windings are connected so that a single interrogation pulse checks two adjacent cores simultaneously, one for an up-going discrete signal and one for a down-going discrete signal. Basically, the memory operates for both up-going and down-going signals in a coincident current mode; that is, if a discrete signal is turned off, an output is obtained only when the core is interrogated for a down-going discrete. Since the memory is preprogramed to interrogate the N1 core for a down-going signal when the Nth core is interrogated for an up-going signal, only one driving circuit per core is needed.

The discrete input to each core is obtained by applying an input from the discrete source through a Schmitt trigger and a discrete driver to the discrete input winding of the core. The discrete signal inputs to the memory usually come from relay contacts, which have inherent mechanical bounce because of spring and mass. This produces an ac signal on the leading and trailing edges of the discrete signal. To absorb the effects of contact bounce, the Schmitt trigger with an integrator on its input is inserted between each discrete source and the respective discrete driver. Only a slight integration is needed because of the hysteresis characteristics of the Schmitt trigger. Therefore, the resolution and reproducibility of the timing between relay excitation and pull-in of the Schmitt trigger are improved. Although the reliability of the memory is somewhat degraded by the introduction of active components, the Schmitt trigger is a very simple and stable circuit and can be designed with a very long mean-time-between-failure factor.

Since it is impractical to operate two cores of the memory simultaneously on one sense winding to derive useful information, one sense winding links all the odd numbered cores and another links all the even numbered cores. Consequently, any two adjacent cores are on different sense lines.

The operation of an individual memory core may be explained by referring to Figure 7 which shows a highly idealized hysteresis loop and the driving current for the core. When a discrete signal is not present, the flux content of the core rests at point A. Any signal from the interrogation source drives the flux within the range of points G, A, and B. This flux change is small; therefore, a small output voltage results.

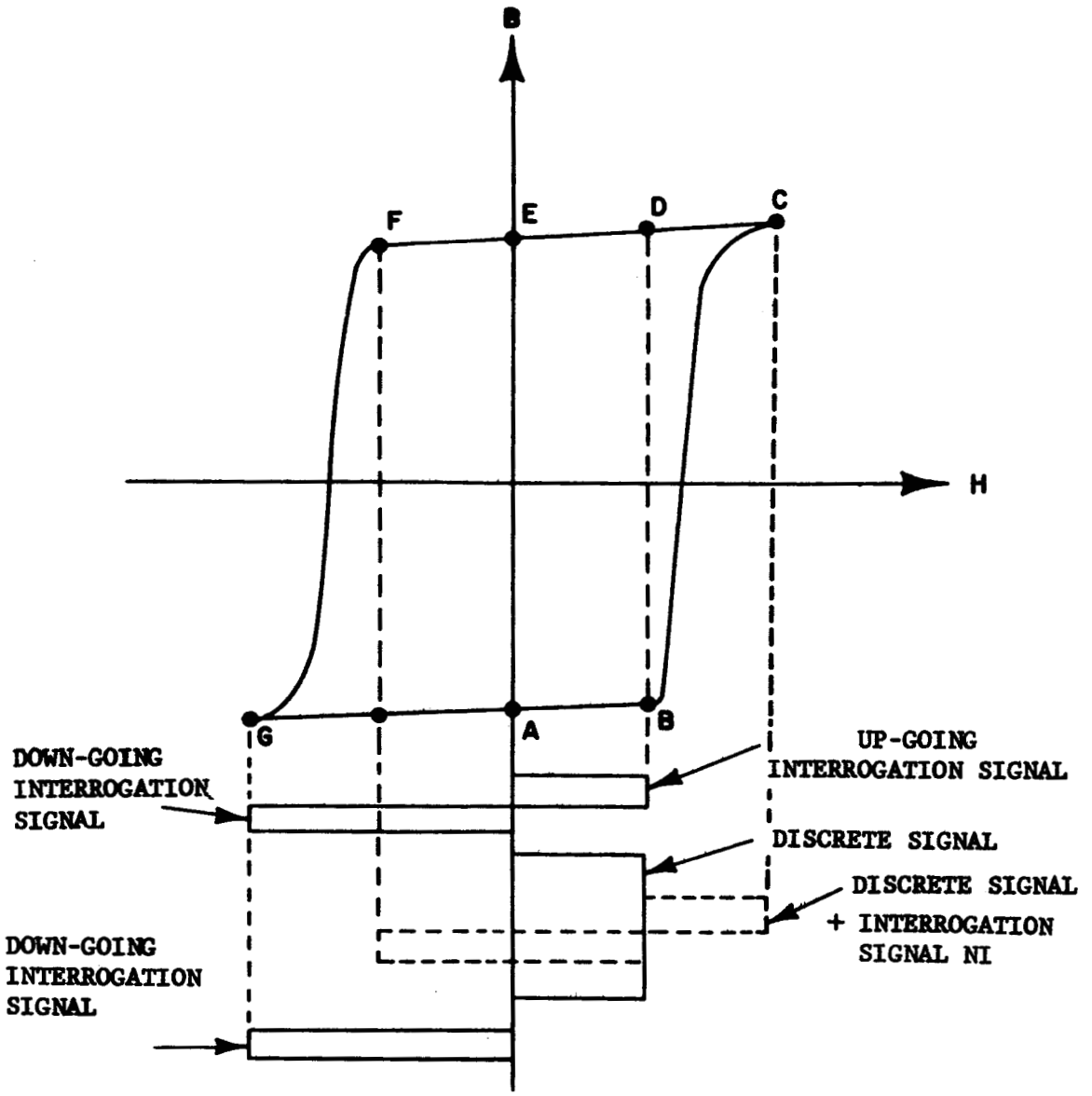

FIGURE 7. IDEALIZED HYSTERESIS LOOP CURVE

If a discrete signal is turned on and maintained, the core is biased to point B. When the next up-going interrogation pulse is applied to the core, its magnetomotive force is added algebraically to the

magnetomotive force of the discrete signal and drives the core to point C. This large flux change results in a large up-going output signal on the sense winding. This output signal is picked up and amplified by the sense amplifier. When the up-going interrogation pulse is removed, the core flux drops to point D. As long as the discrete signal is applied to the core, the interrogation pulses drive the flux in the range of points F, E, D, and C. This results in very small output pulses, or noise, on the sense winding. Signal-to-noise ratios of 8 to 1 or 10 to 1 are common, so detection is not a problem. When the discrete signal is removed, there is zero net magnetomotive force on the core, and the flux content drops to point E. When the next down-going interrogation pulse is applied, the net magnetomotive force is sufficient to drive the core to point G. This results in a down-going output from the sense winding which is equal in amplitude but opposite in polarity to an up-going output signal.

It should be noted that an output is obtained from a core only when there is a change in the discrete signal. Therefore, information is applied to the computer only for changes in discrete signals.

5. Ground Commutator. The ground commutator (Fig. 8) is basically a Johnson shift register utilizing Texas Instrument micrologic modules operating on a 50-percent duty cycle. The commutator is driven by the last phase of the eight-phase driver. Its function is to turn on the power amplifiers in the discrete drivers prior to interrogation of memory cores and to turn them off after interrogation. At any one time, only one-fourth of the discrete drivers can be on.

If a condition existed in which all the discrete drivers in all the memory units were on at the same time and remained on continually, the maximum input power required to drive the system would be excessive. Therefore, the ground commutators (one per memory unit) are employed to reduce this requirement by 75 percent. The discrete driver amplifiers of the memory are mounted in groups of 16 with a common return line to ground. This return to ground is interrupted by the output of the commutator. To turn on these amplifiers, the common return line is grounded by the ground commutator. To prevent a discrete amplifier from being turned on at the same time its memory core is interrogated, a second group of 16 cores is enabled by the commutator. This ensures that there is an overlap in the turning on and turning off of the various groups of discrete drivers. The logic used ensures an overlap of at least eight discrete amplifiers as they are scanned. By turning on only two groups of 16 in each memory unit, a 75 percent power reduction is achieved.

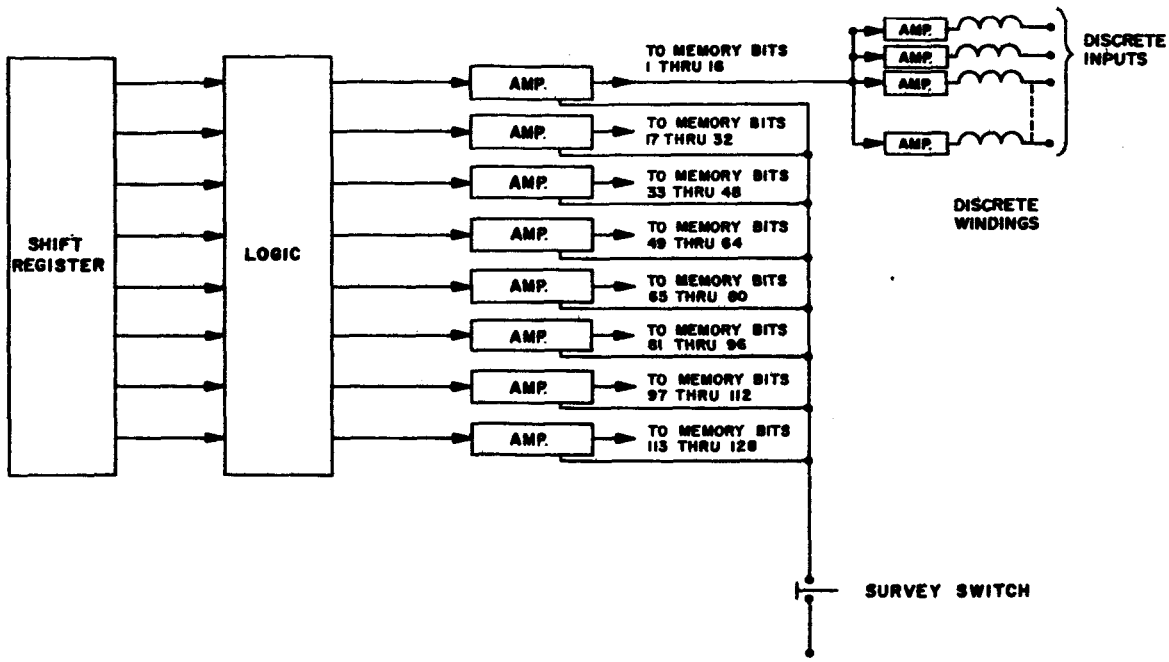

FIGURE 8. GROUND COMMUTATOR BLOCK DIAGRAM

6. Sense Amplifier. The sense amplifier (Fig. 9) separates the up-going and down-going signals coming from the memory bank. One pair of Darlington amplifiers separates the up-going and down-going signals from the odd-core sense windings, while the signals from the even-core sense windings are separated by another pair.

In each pair, the Darlington amplifiers are driven by signals of opposite polarity obtained from the center-tapped secondary windings of a transformer. With this type input, one amplifier processes only the up-going signals while the other processes only the down-going signals.

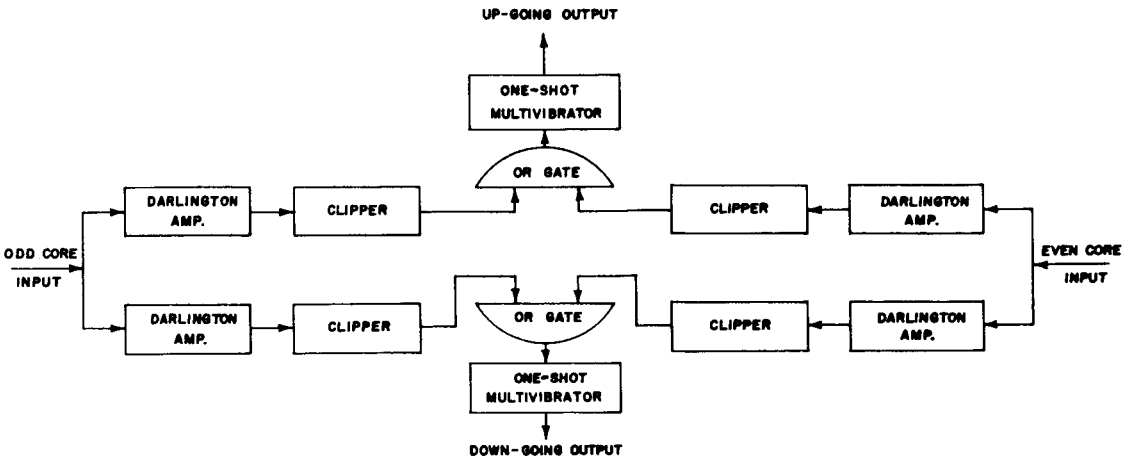

FIGURE 9. SENSE AMPLIFIER BLOCK DIAGRAM

The output of each Darlington amplifier is fed to a clipper for noise suppression. At the output of the clipper, all up-going signals are fed to one OR gate and all down-going signals are fed to another OR gate. The output of each OR gate triggers a one-shot multivibrator that supplies inputs to the system register.

E. ENCODER CIRCUIT

The encoder circuit (Fig. 10) consists of the system register, OR gate, priority interrupt, read driver, clock stopper, and clock-start multivibrator.

1. System Register. The system register serves as the interface between the discrete activity indicator system and the computer. Inputs are received from the sense amplifiers and the binary counter for transfer to the computer.

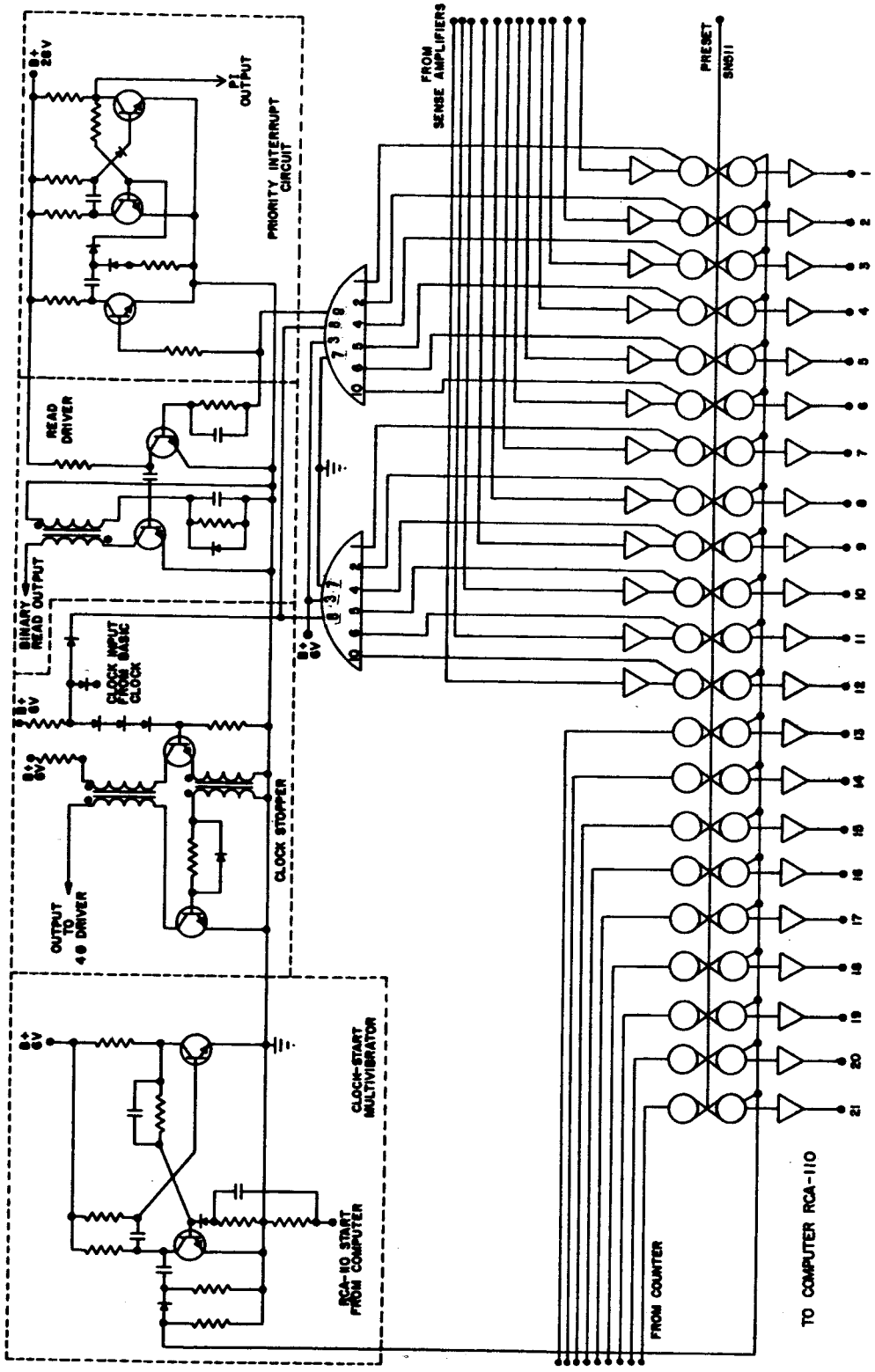

FIGURE 10. ENCODER CIRCUIT DIAGRAM

Since it is possible for each amplifier to supply both an up-going and a down-going signal, 12 inputs may be supplied to the register from the sense amplifiers. Each of these inputs is applied through an amplifier (for isolation) to a bistable multivibrator. The output of the multivibrator passes through an inverter to the computer register and to an OR gate. These outputs tell the computer in which memory unit the discrete signal change occurred and the direction of the change.

The binary counter supplies inputs to seven bistable multivibrators in the system register, one input coming from each counter stage. This total input represents the binary count and tells the computer which discrete signal changed in the memory unit.

2. OR Gate. The OR gate drives the priority interrupt circuit, the read driver, and the clock stopper.

3. Priority Interrupt. The static output of the OR gate drives the priority interrupt circuit, which is the one-shot multivibrator. The output of the multivibrator is a 130-μs pulse that is required as the priority interrupt signal for the RCA-110 computer. The priority interrupt pulse alerts the computer that new information is contained in the system register and is ready to be written into one of the computer's registers.

4. Read Driver. The static output of the OR gate also drives the blocking-oscillator read driver. This blocking oscillator supplies a read pulse (at approximately γ time) to the small aperture in the bottom cores of the binary counter. Outputs of the binary counter are then gated into the register.

5. Clock Stopper. The clock stopper is essentially an AND gate. The output of the basic clock is gated through this AND gate, provided the static input from the OR gate is not present. When the input from the OR gate is absent, the input from the basic clock drives an amplifier, which, in turn, drives a blocking oscillator. The insertion of the blocking oscillator here, as in several other instances in this system, merely changes the output from voltage-driven to current-driven. This output of the blocking oscillator drives the functional clock. When the output of the OR gate is present, it shunts the basic-clock signal to ground, disabling the blocking oscillator. The system stops scanning, allowing information to be received and processed by the computer.

6. Clock-Start Multivibrator. After the computer has processed the information, a pulse from the computer operates the clock-start multivibrator, which resets all bistable multivibrators in the system register. By removing the OR gate signal, the system is allowed to resume scanning.

F. SURVEY SWITCH

The survey switch allows the system operator to observe by computer printout any condition that exists in all the 768 discrete inputs at any one time.

When the survey switch is pressed, it removes B+ from the ground commutator. This removes discrete inputs from all memory cores. When the memory cores are interrogated, a down-going signal is produced, but only if there had been a discrete input present before the survey switch was pressed. When the B+ has been re-applied, there is an output on the first scan cycle for each discrete input. Since this would produce the desired information twice, and thereby tie up the computer longer, the removal of B+ also disables the sense amplifier in each memory unit. Therefore, the only information presented to the computer is that produced by the first scan when B+ is replaced on the ground commutator.

G. BINARY SYNCHRONIZER

The discrete activity indicator system does not have a positive means of synchronization once it has started scanning. Therefore, the binary synchronizer is incorporated to re-establish synchronization automatically if the system loses synchronization because of loss or gain of a count.

Figure 11 is a schematic diagram of the binary synchronizer, which is essentially a sequential AND gate. In operation, if winding N2 is not energized between the time that windings N1 and N3 are energized, a blocking oscillator is triggered. Windings N1, N2, and N3 are wound on a square-loop core; windings N4, N5, and N6 are wound on a linear core. Windings N5 and N6, along with the transistor, form the blocking oscillator which, when triggered, drives the system reset.

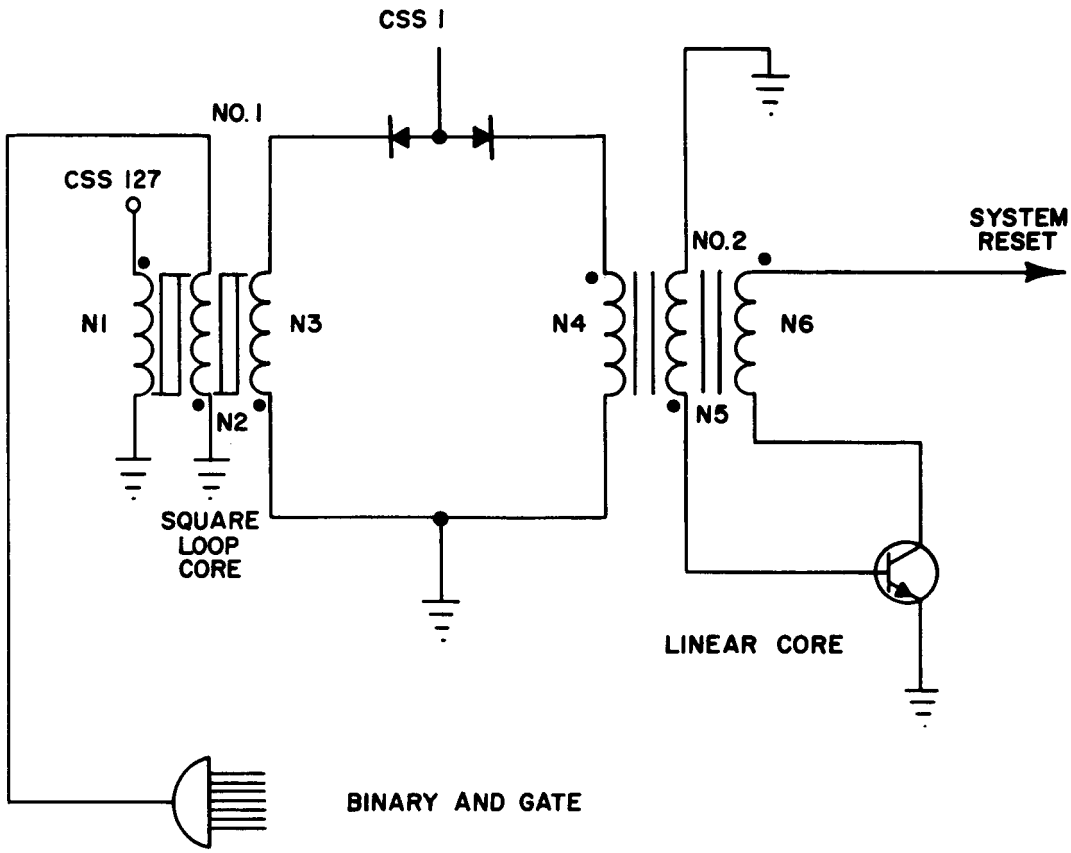

FIGURE 11. BINARY SYNCHRONIZER

If the system is synchronized, the first pulse to the square-loop core comes from current-steering switch output No. 127. This pulse is applied to winding N1 and switches the core. The next pulse is fed to winding N2 from the binary AND gate (only if count 128 is in the binary counter) to switch the square-loop core back to its original condition. The third pulse comes from current-steering switch output No. 1 and is applied to winding N3. Since the square-loop core is already reset, the impedance of winding N3 is very low and most of the current is shunted through winding N3. The current that

passes through winding N4 is insufficient to trigger the blocking oscillator. Hence, nothing happens and the system is allowed to continue scanning.

If the system is out of synchronization, the first pulse to winding N1 from current-steering switch output No. 127 switches the square-loop core. The pulse from the binary AND gate is not present because of loss of synchronization. Then the pulse from current-steering switch output No. 1 is applied through winding N3, which now has a high impedance, and resets the square-loop core. Under these conditions, sufficient current flows through winding N4 to trigger the blocking oscillator, which then drives the system reset.

At reset, the system goes to the starting point. An extra winding is added to all cores of the binary counter, the current steering switches, the eight-phase drivers, and the functional clock to switch these cores to the starting position.

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DISCRETE ACTIVITY INDICATOR SYSTEM

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The information in this report has been reviewed for security classification. Review of any information concerning Department of Defense or Atomic Energy Commission programs has been made by the MSFC Security Classification Officer. This report, in its entirety, has been determined to be unclassified.

This document has also been reviewed and approved for technical accuracy.

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